N+ substrate, special attention must be given to the voltage applied to the substrate, which is no longer isolated from the high potential of the power supply. Alternatively, the FIG. **10** structure can be built on an N+/Buried Oxide/Silicon foundation.

[0040] FIG. **11** shows another alternate embodiment of a PSIT **1100**. The PSIT **1100** comprises a lightly-doped p-type epitaxial layer formed on a P+ semiconductor (e.g., silicon) substrate **1104**. Spaced-apart gate regions in the form of N-type wells (NW) **1106** are formed in the epitaxial layer **1102**. P-type source regions **1108** are formed in the epitaxial layer **1102** between the gate regions **1106**. A P-type drain region in the form of a P-well (PW) **1110** is formed in the epitaxial layer **1102** and spaced-apart from the source regions **1108** to define a channel region therebetween. Dielectric (e.g., shallow trench isolation (STI) silicon oxide) carrier separation layers **1112** are formed at the periphery of the gate regions **1106**. In the FIG. **11** embodiment, STI regions **1114** are also formed at the periphery of the drain region **1110**. In the FIG. **11** PSIT **1100**, the drain region **1110** is relatively large to minimize contact resistance to the substrate.

[0041] FIG. **12** shows another alternate embodiment of a PSIT **1200**. The PSIT **1200** comprises a lightly-doped p-type epitaxial layer **1202** formed on P+ semiconductor (e.g., silicon) substrate **1204**. Spaced-apart gate regions in the form of N-type wells (NW) **1206** are formed in the epitaxial layer **1202**. P-type source regions **1208** are formed in the epitaxial layer **1202** between the gate regions **1206**. A P-type drain region in the form of a P-sinker region **1210** is formed in the epitaxial layer **1202** and spaced-apart from the source regions **1208** to define a channel region therebetween. Dielectric (e.g., shallow trench isolation (STI) silicon oxide) carrier separation layers **1212** are formed at the periphery of the gate regions **1206**. In the FIG. **12** embodiment, STI regions **1214** are also formed at the periphery of the drain region **1210**. The P-sinker region **1210** may be implemented as a combination of p-well or "sinker down" for the top portion of the epi, and "sinker up" for the bottom portion.

[0042] FIG. **13** shows another alternate embodiment of a PSIT **1300**. The PSIT **1300** comprises a P-buried layer (PBL) **1302** formed in a lightly-doped p-type semiconductor (e.g., silicon) substrate **1304**. Spaced-apart gate regions in the form of N-wells (NW) **1306** are formed in the substrate **1304** above the P-buried layer **1302**. P-type source regions **1308** are formed in the substrate **1304** between the gate regions **1306**. A P-type drain region in the form of P-sinker region **1310** is formed in the substrate **1304** and spaced-apart from the source regions **1308** to define a channel region therebetween. Dielectric (e.g., shallow trench isolation (STI) silicon oxide) carrier separation layers **1312** are formed at the periphery of the gate regions **1306**. In the FIG. **13** embodiment, STI regions **1314** are also formed at the periphery of the drain region **1310**. Since this embodiment uses a P-type substrate that is not isolated from the drain region at the surface of the die, special attention must be given to the voltage applied to the substrate, or the substrate is used as a secondary drain electrode. Alternatively, the structure may be built on a P+/Buried Oxide/Silicon foundation.

[0043] It should be understood that the particular embodiments of the subject matter described above have been provide by way of example and that other modifications may occur to those skilled in the art without departing from the scope of the claimed subject matter as expressed in the appended claims and their equivalents.

1. A static induction transistor comprising:

a region of semiconductor material having a first conductivity type;

at least two spaced-apart gate regions formed in the region of semiconductor material, the gate regions having a second conductivity type that is opposite the first conductivity type;

at least one source region having the first conductivity type formed in the region of semiconductor material between the spaced-apart gate regions;

a drain region having the first conductivity type formed in an upper surface of the region of semiconductor material and spaced-apart from the source region to define a channel region therebetween; and

a dielectric carrier separation layer formed at the periphery of each gate region.

2. The static induction transistor of claim **1**, wherein the dielectric carrier separation layers are spaced-apart by a distance d that is greater than or equal to $2W_{D0}$, wherein W_{D0} equals depletion layer thickness at $V_{GS}=0$.

3. The static induction transistor of claim **1**, wherein the first conductivity type is P-type and the second conductivity type is N-type.

4. The static induction transistor of claim **1**, wherein the first conductivity type is N-type and the second conductivity type is P-type.

5. A static induction transistor (SIT) comprising:

a P-type silicon substrate having an upper surface;

a deep N-type well region formed in the P-type silicon substrate;

a plurality of spaced-apart P-type well regions formed in the deep N-type well region, each P-type well region having a P+ region formed at an upper surface thereof to define a P-type gate region of the SIT;

at least one N+ source region formed at the upper surface of the deep N-type well between adjacent P-type gate regions;

an N-type well region formed in the upper surface of the P-type silicon substrate at the periphery of the deep N-type well region, the N-type well region having an N+ region formed at an upper surface thereof to define a drain region of the SIT; and

for each P-type gate region, a dielectric carrier separation layer formed at the periphery of the P-type gate region.

6. The SIT of claim **5**, wherein the at least one N+ source region has a width d that is greater than or equal to $2W_{D0}$, wherein W_{D0} equals the thickness of the SIT depletion layer at $V_{GS}=0$.

7. A method of forming a static induction transistor (SIT) in a region of semiconductor material having a first conductivity type, the method comprising:

forming at least two spaced-apart gate regions in the semiconductor material, the gate regions having a second conductivity type that is opposite the first conductivity type;

forming at least one source region having the first conductivity type in the semiconductor material between adjacent spaced-apart gate regions:

forming a drain region having the first conductivity type in an upper surface of the semiconductor material and spaced-apart from the source region to define an SIT channel region therebetween; and